

FIG.1A

SDRAM: BURST LENGTH=8

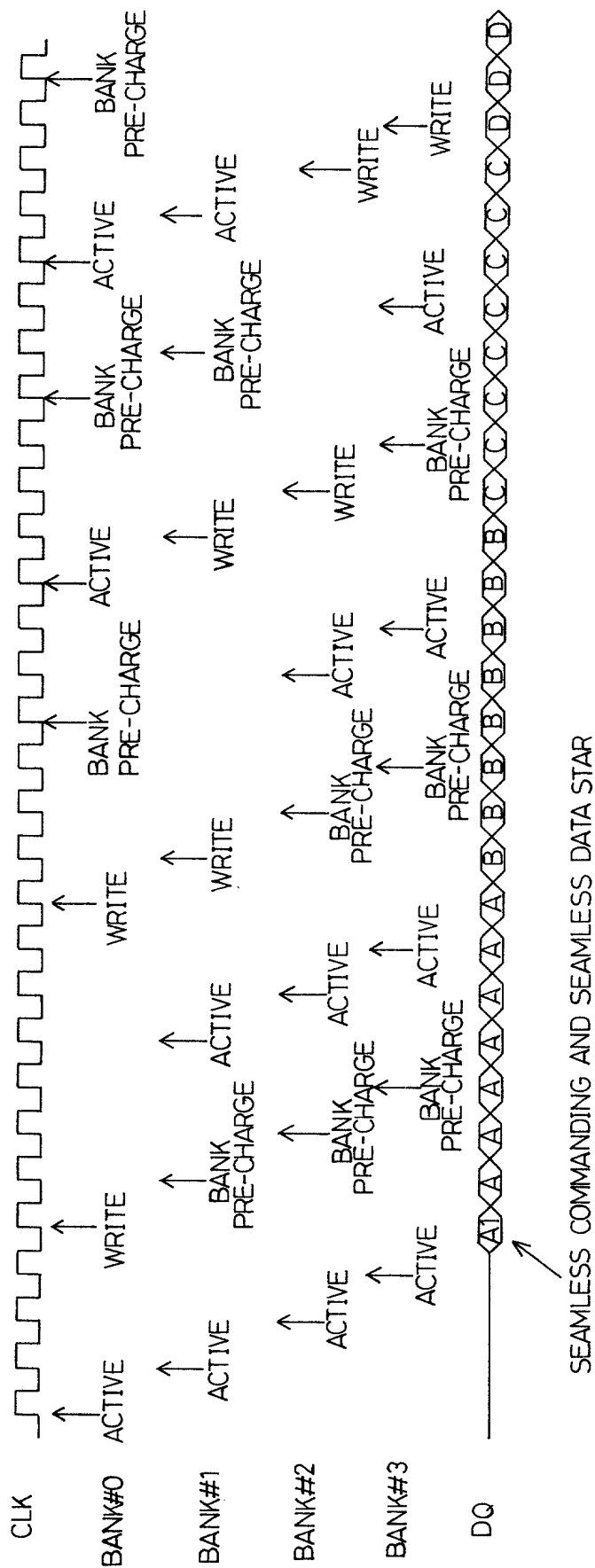


FIG.1C

SDRAM: LATENCY=3; BURST LENGTH=2;

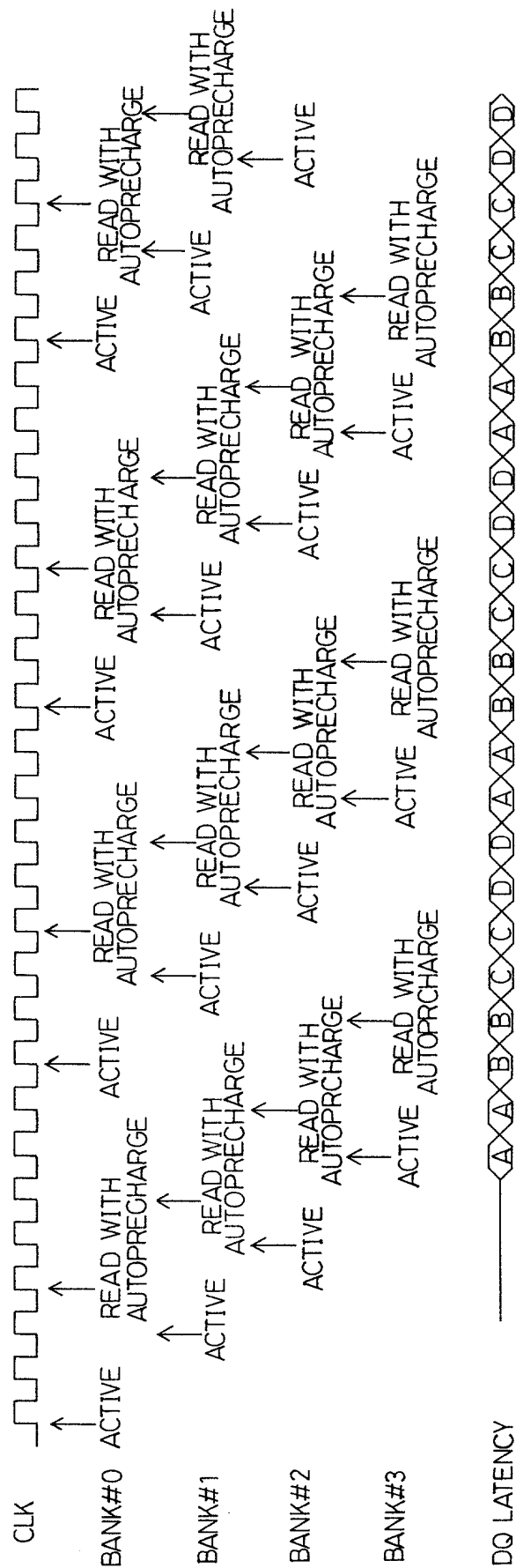


FIG. 2B

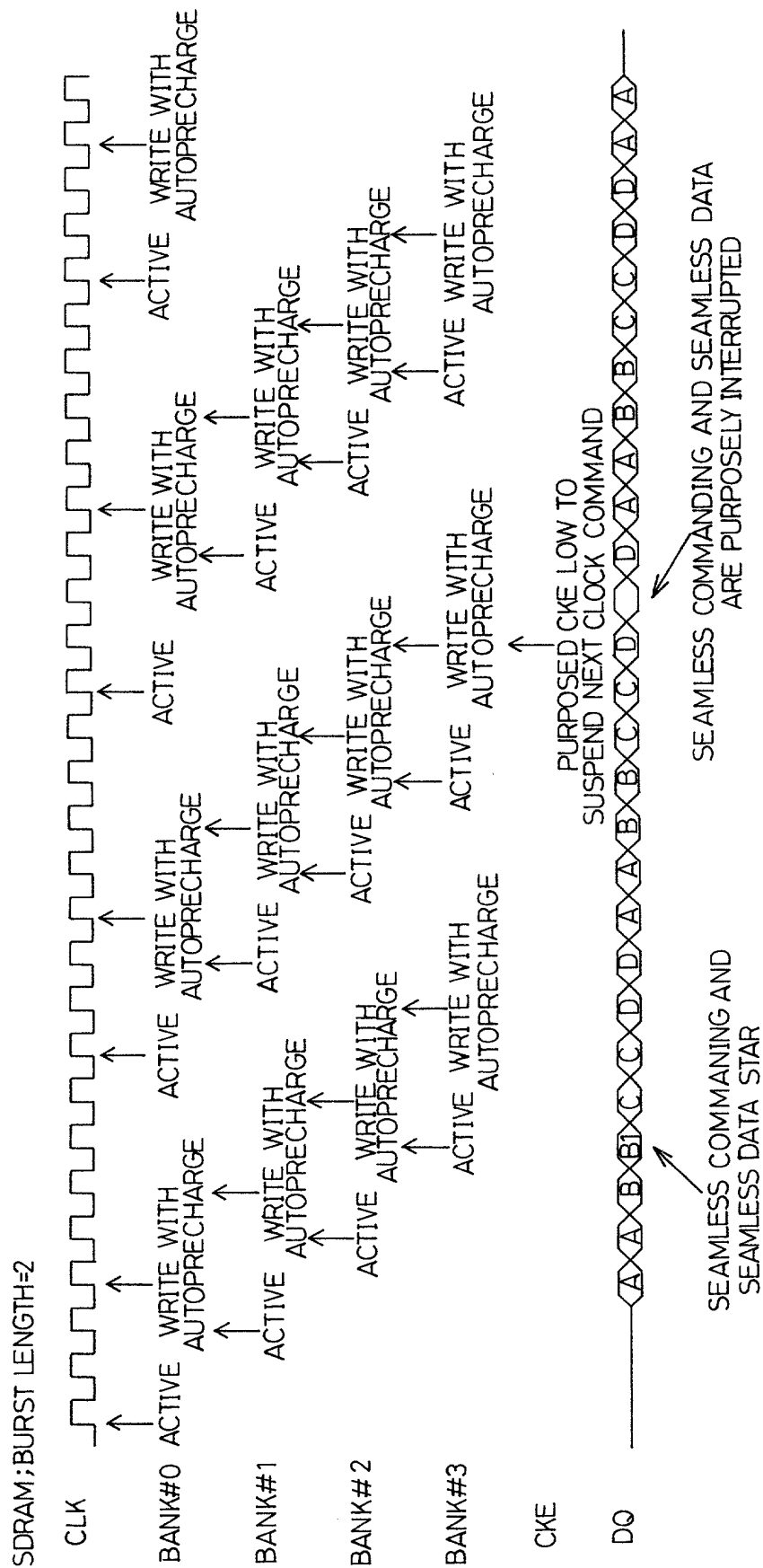
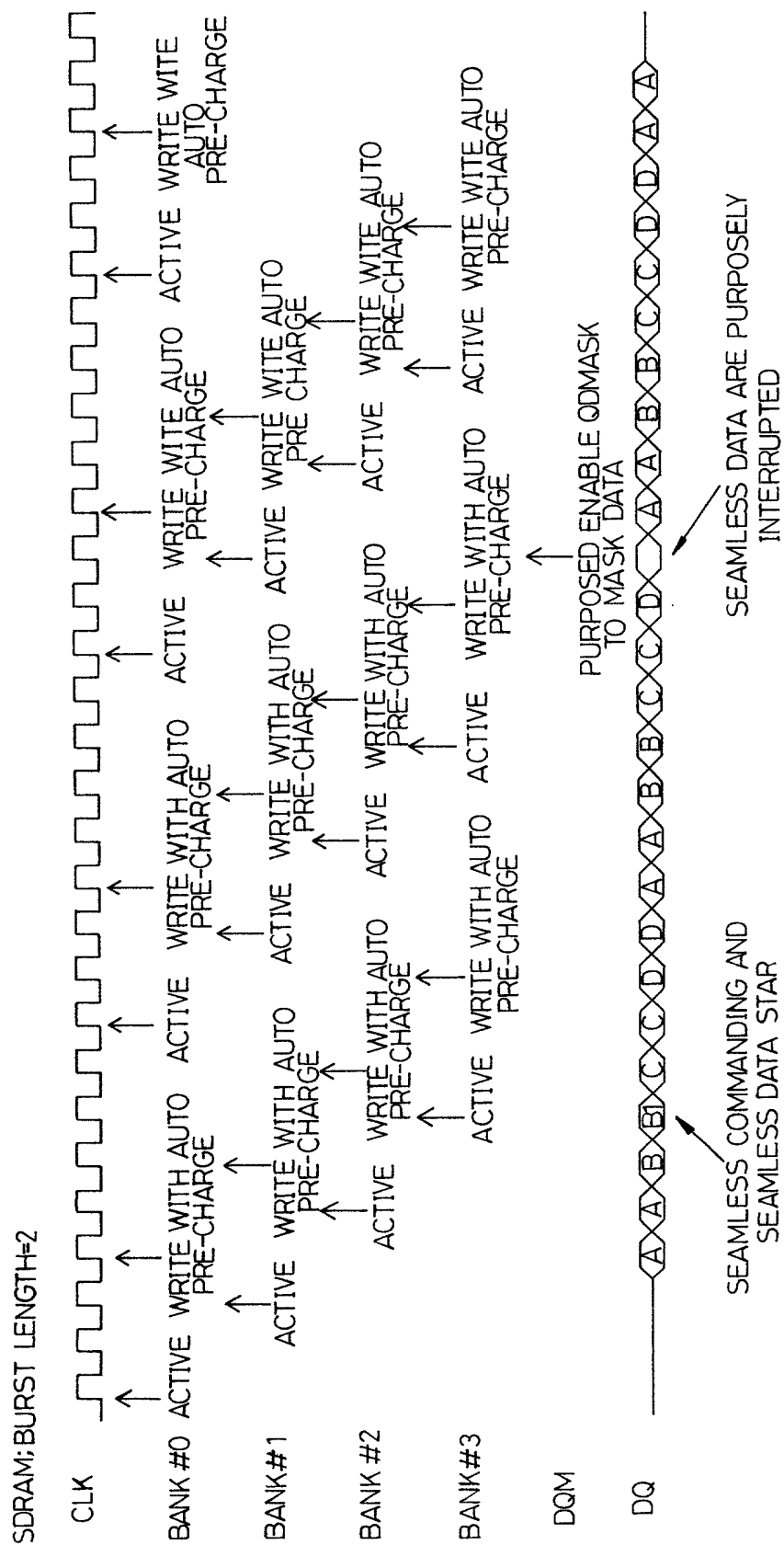


FIG. 2C



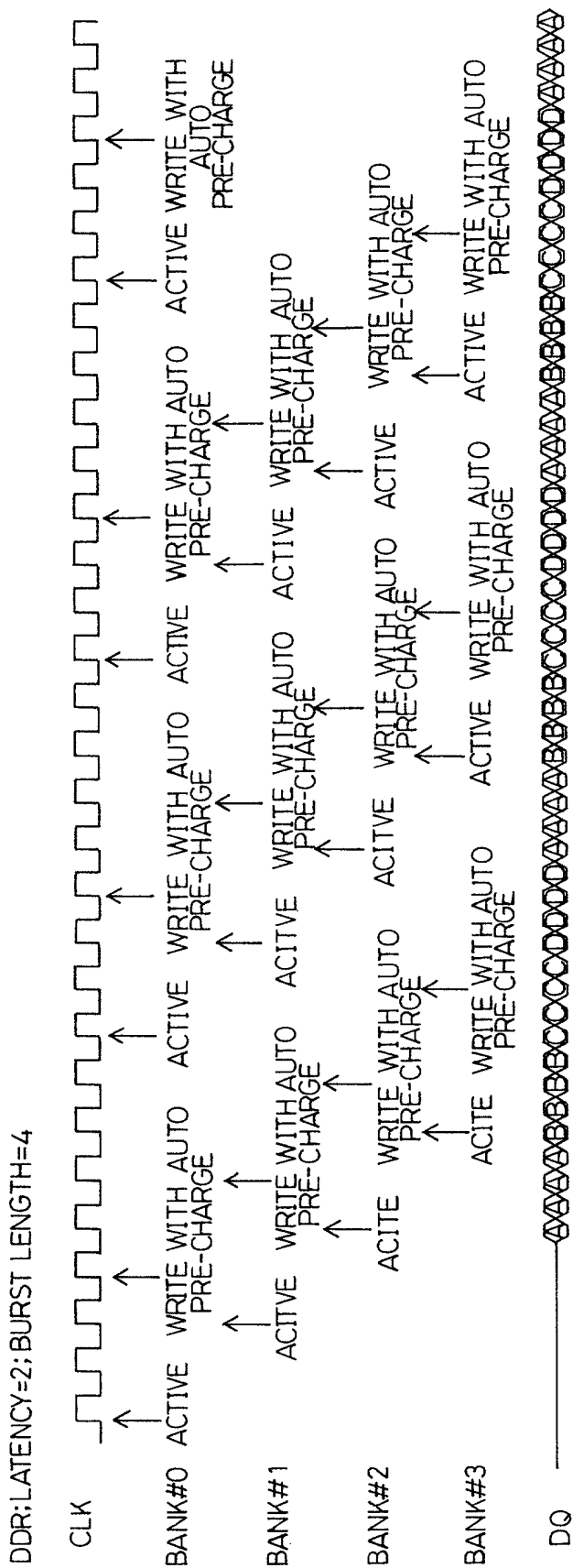


FIG. 3A

DDR: LATENCY=2; BURST LENGTH=4

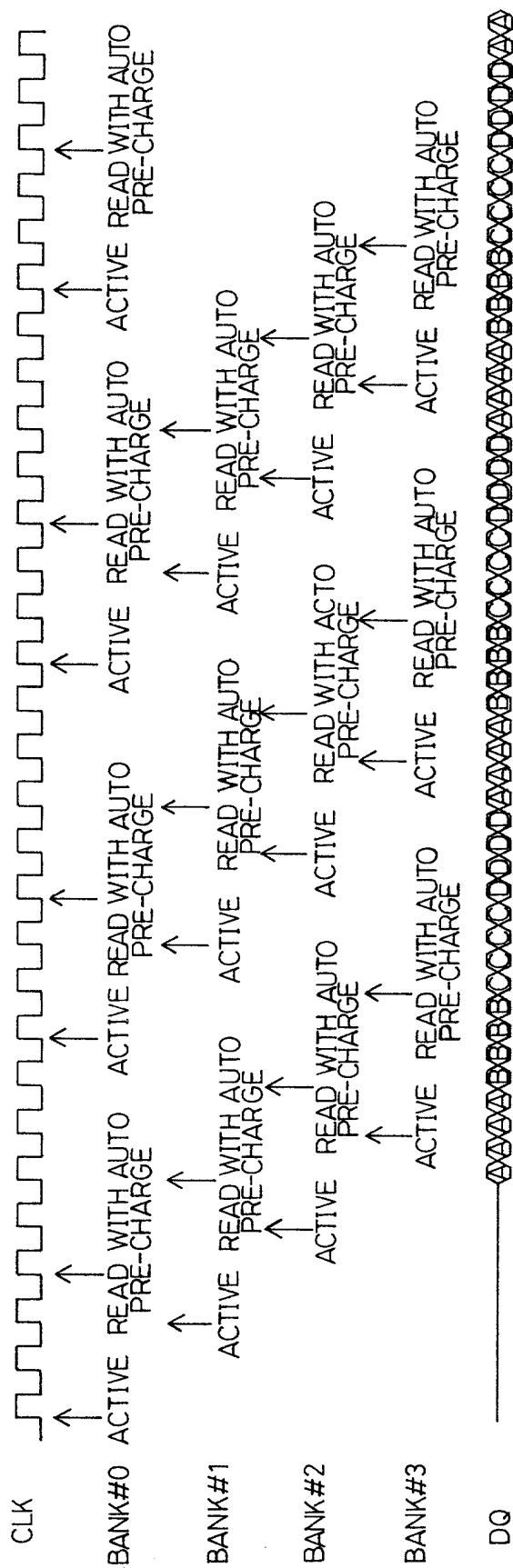


FIG. 3B

TRANSACTION A:	a0 = {Da, Ba, Ra0}	a1 = {Da, Ba, Ca1}	a2 = {Da, Ba, Ca2}	a3 = {Da, Ba, Ca3}	a4 = {Da, Ba, Ca4}
TRANSACTION B:	b0 = {Db, Bb, Rb0}	b1 = {Db, Bb, Cb1}	b2 = {Db, Bb, Cb2}	b3 = {Db, Bb, Cb3}	b4 = {Db, Bb, Cb4}
TRANSACTION C:	c0 = {Dc, Bc, Rc0}	c1 = {Dc, Bc, Cc1}	c2 = {Dc, Bc, Cc2}	c3 = {Dc, Bc, Cc3}	c4 = {Dc, Bc, Cc4}
TRANSACTION D:	d0 = {Dd, Bd, Rd0}	d1 = {Dd, Bd, Cd1}	d2 = {Dd, Bd, Cd2}	d3 = {Dd, Bd, Cd3}	d4 = {Dd, Bd, Cd4}
TRANSACTION E:	e0 = {De, Be, Re0}	e1 = {De, Be, Ce1}	e2 = {De, Be, Ce2}	e3 = {De, Be, Ce3}	e4 = {De, Be, Ce4}

RDRAM:TRR=8 TCYCLE;TCAC=8 TCYCLE;TRAS=20 TCYCLE;TRDP=4 TCYCLE;

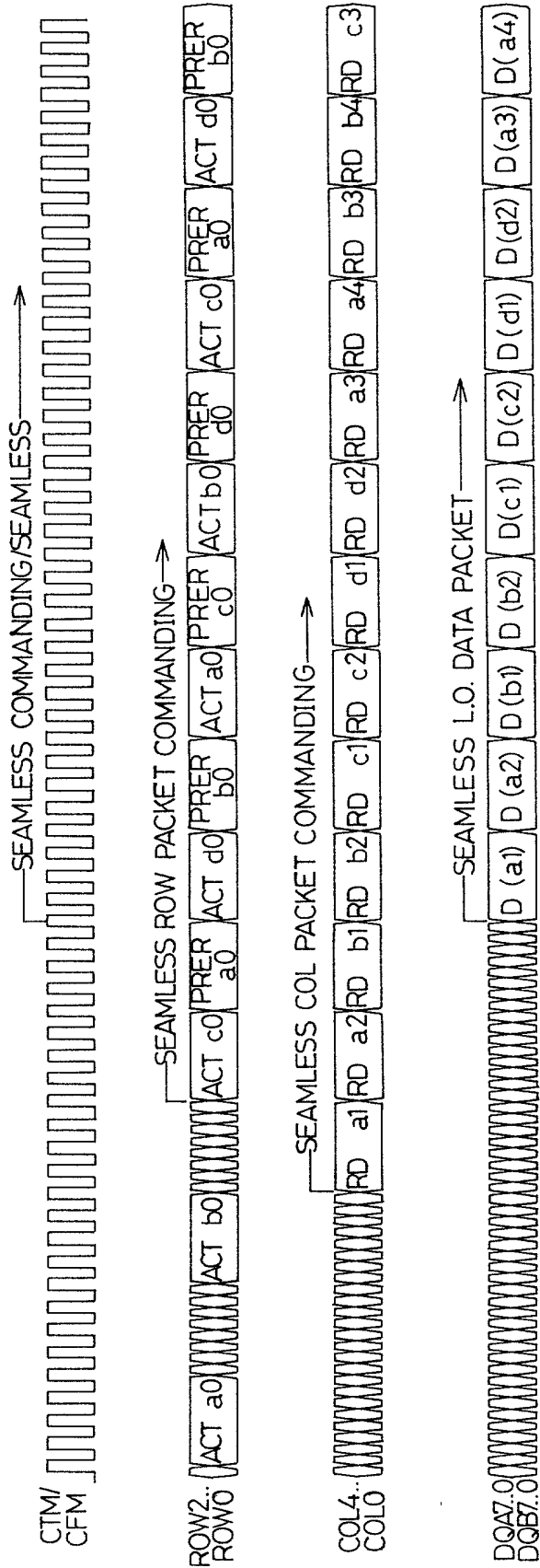


FIG.4B

SDRAM: BURST LENGTH=4

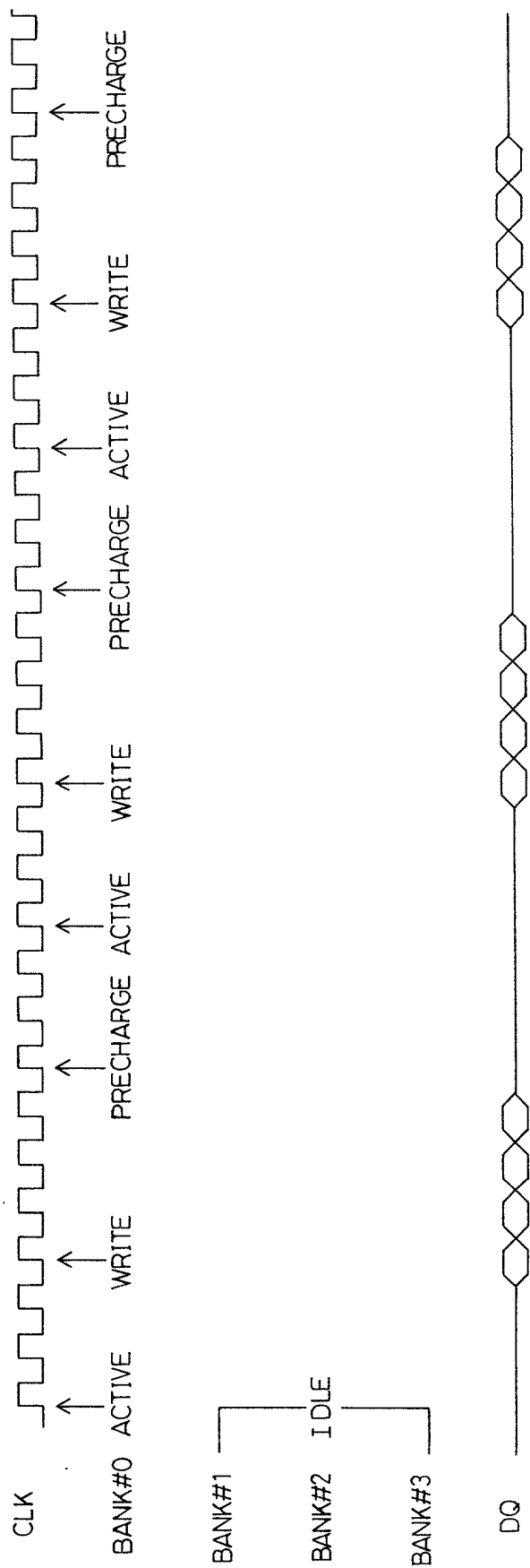


FIG. 5
PRIOR ART

SDRAM; LATENCY=2; BURST LENGTH=4

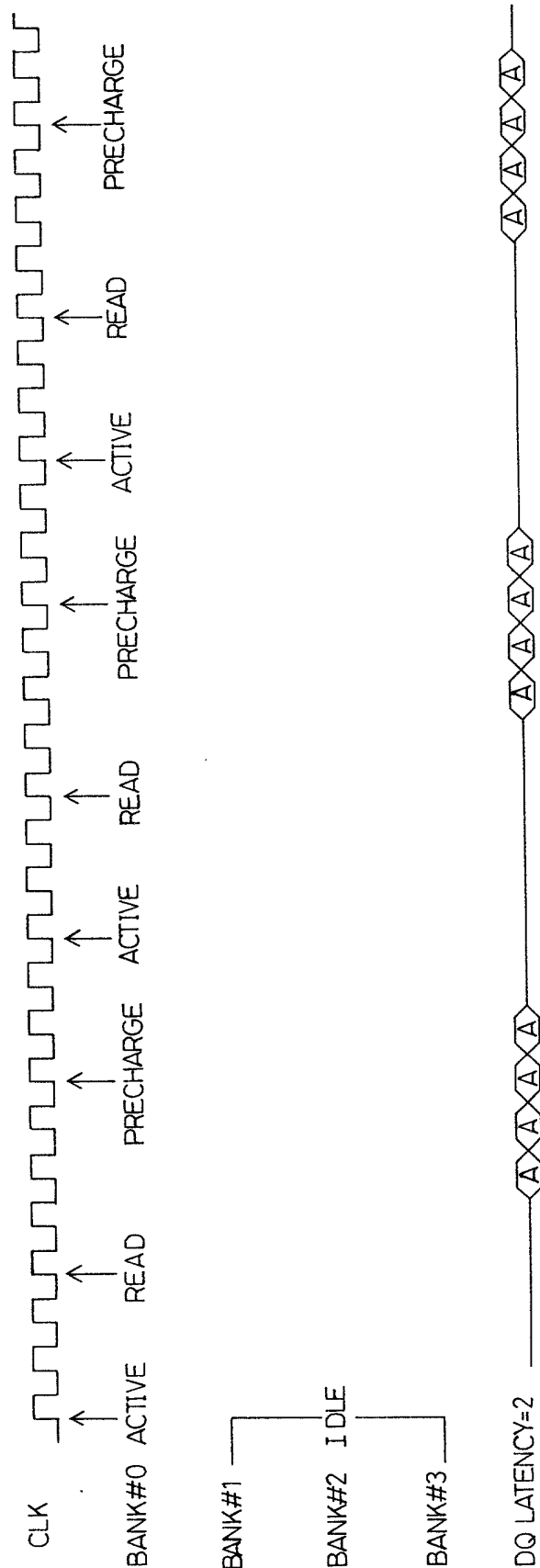


FIG. 6A
PRIOR ART

SDRAM; LATENCY=3; BURST LENGTH=4

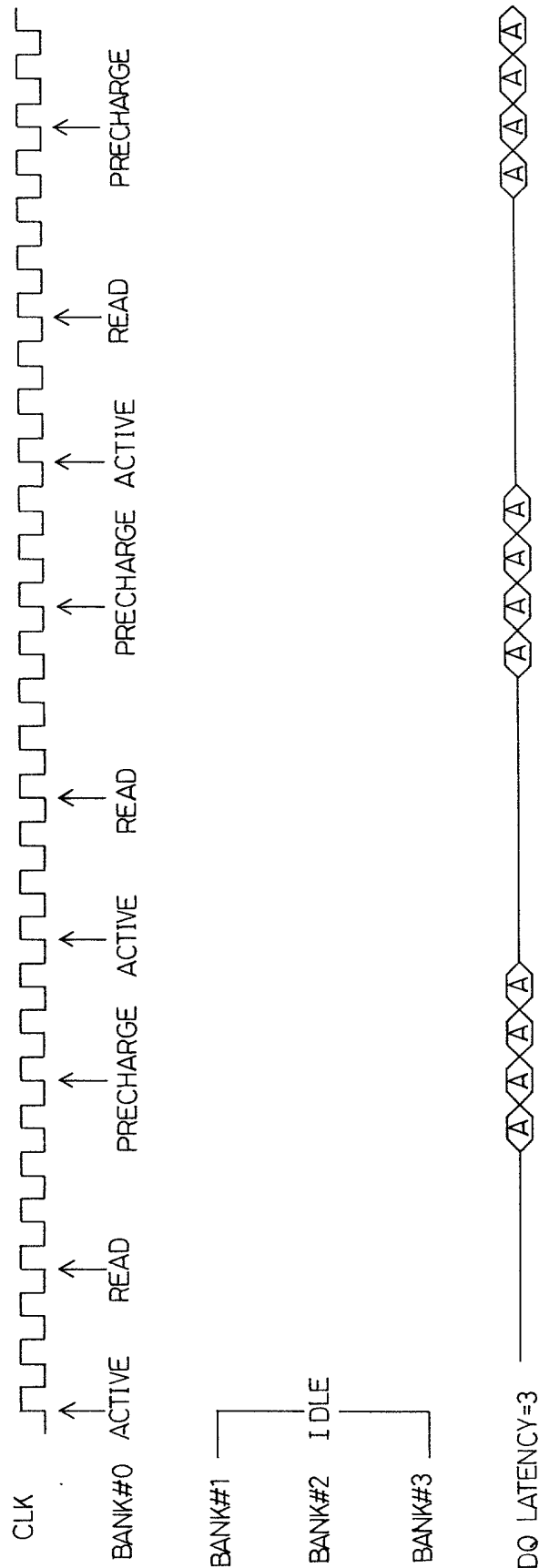


FIG. 6B
PRIOR ART

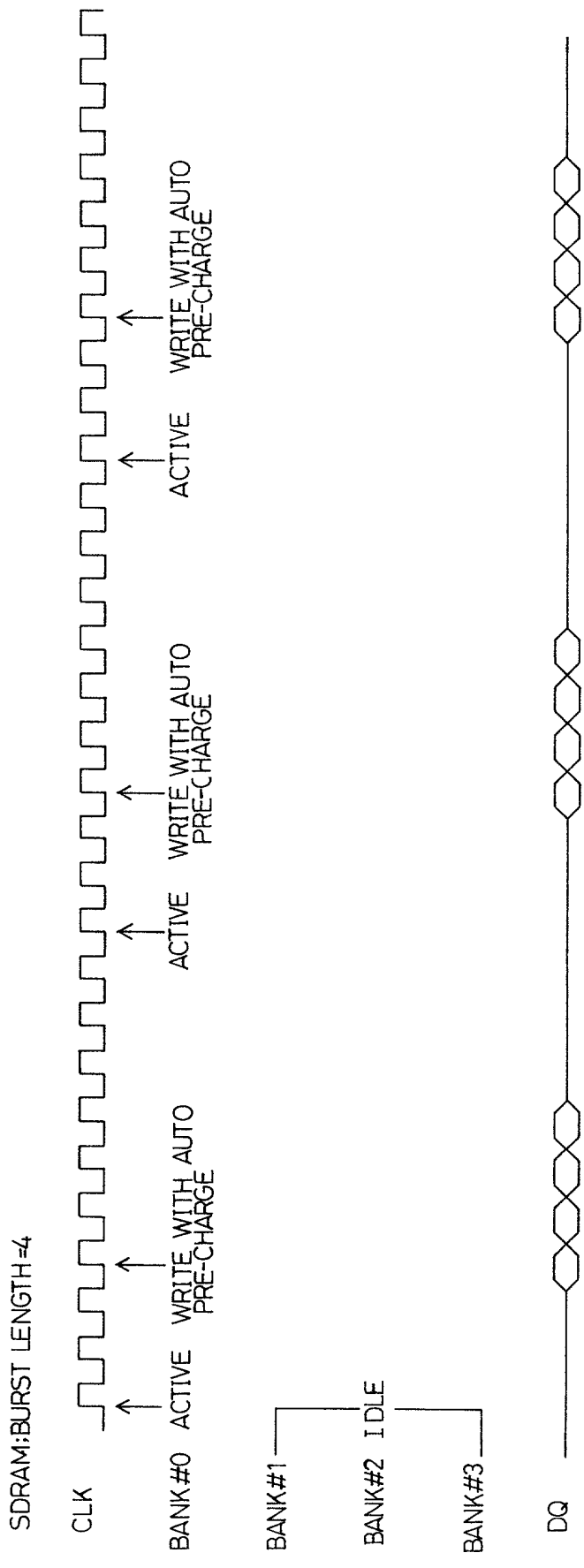


FIG. 7
PRIOR ART

SDRAM: LATENCY=2; BURST LENGTH=4

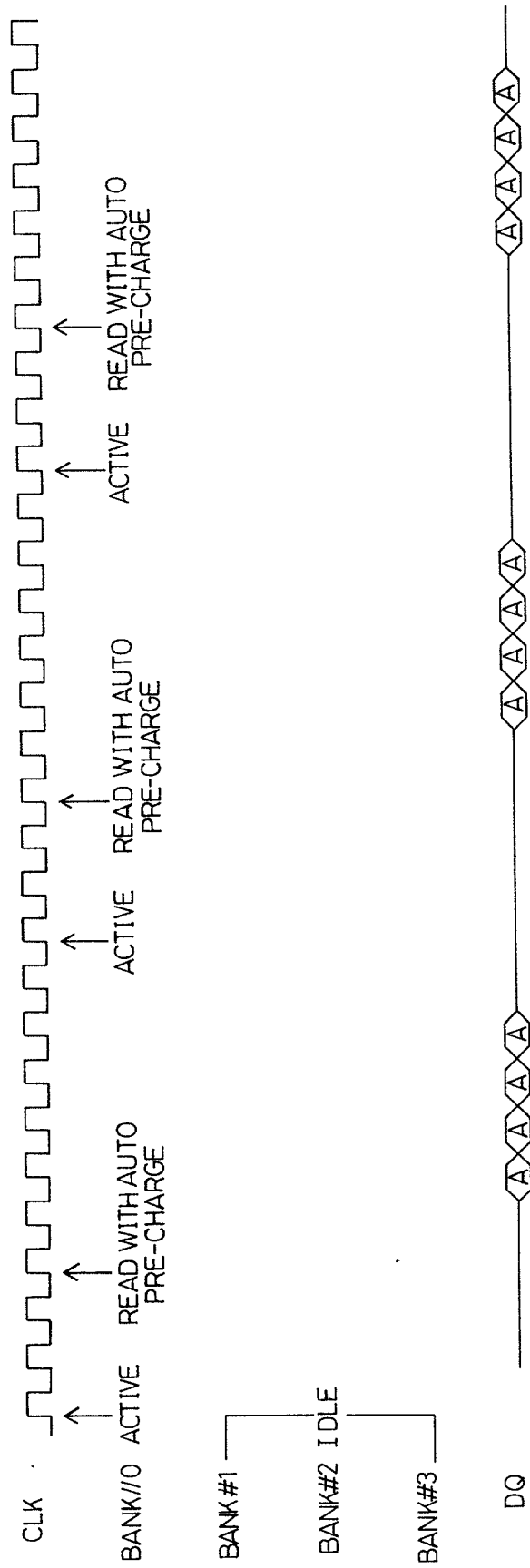


FIG. 8A
PRIOR ART

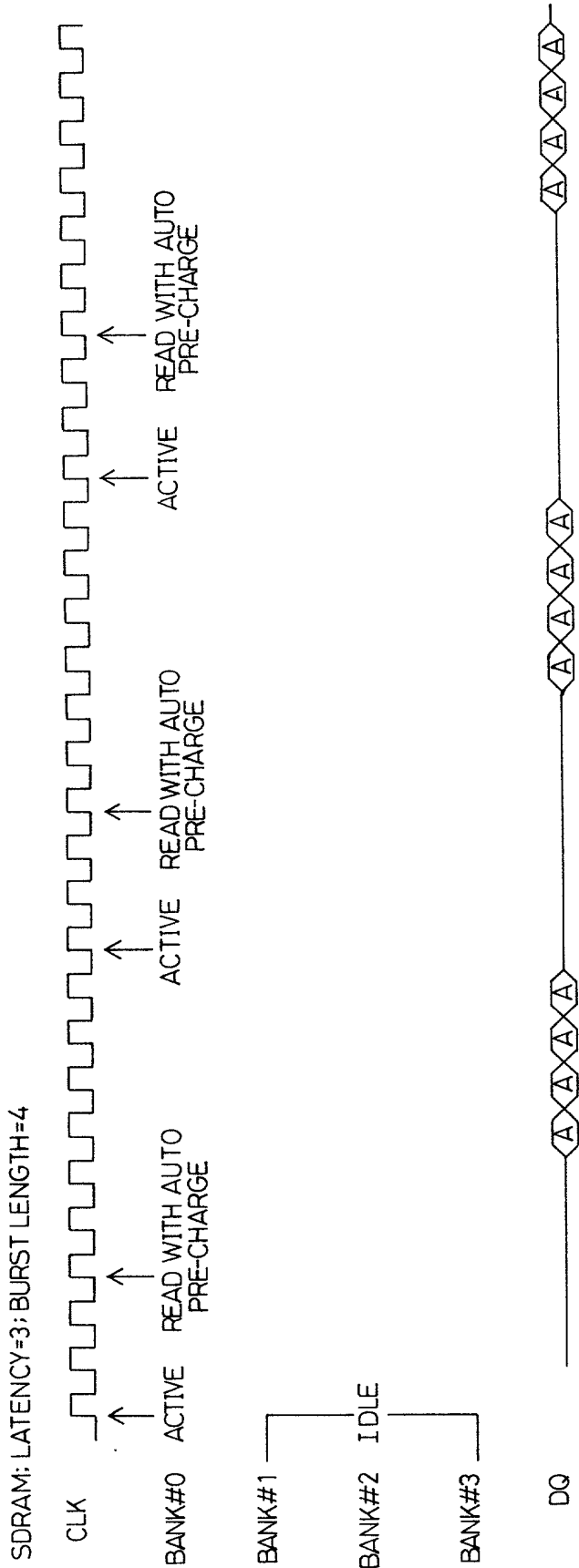


FIG. 8B
PRIOR ART

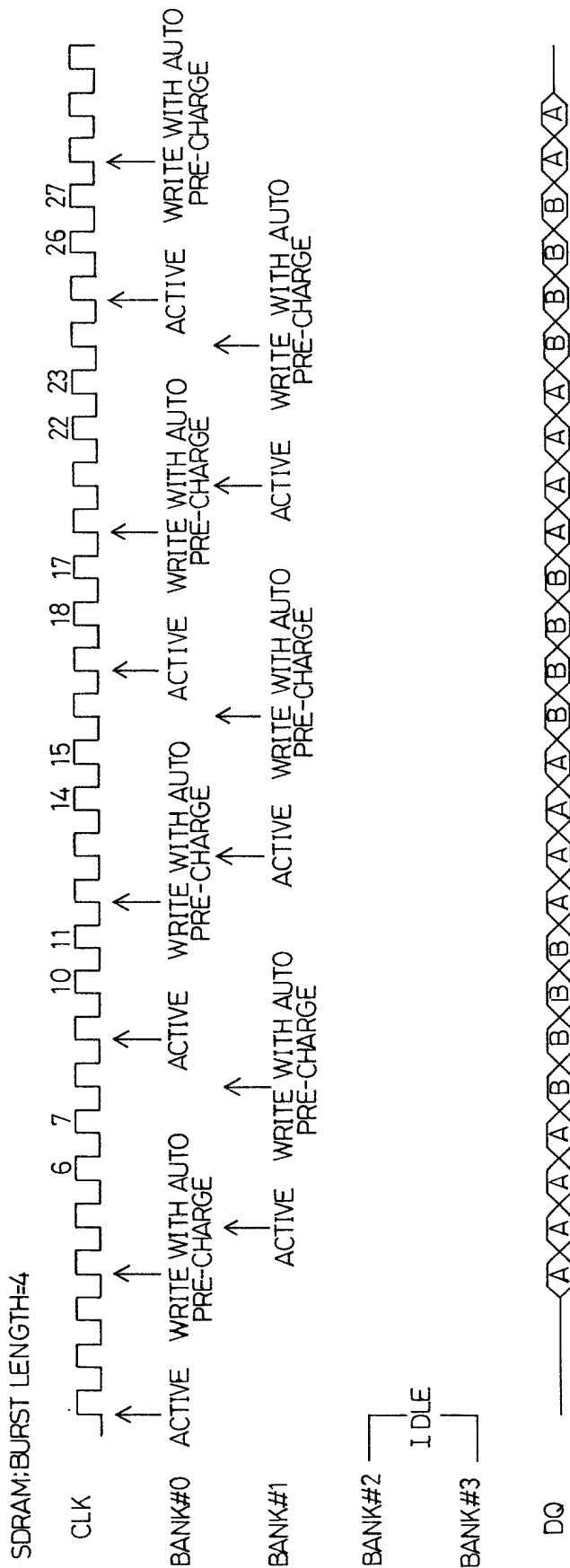


FIG. 9
PRIOR ART

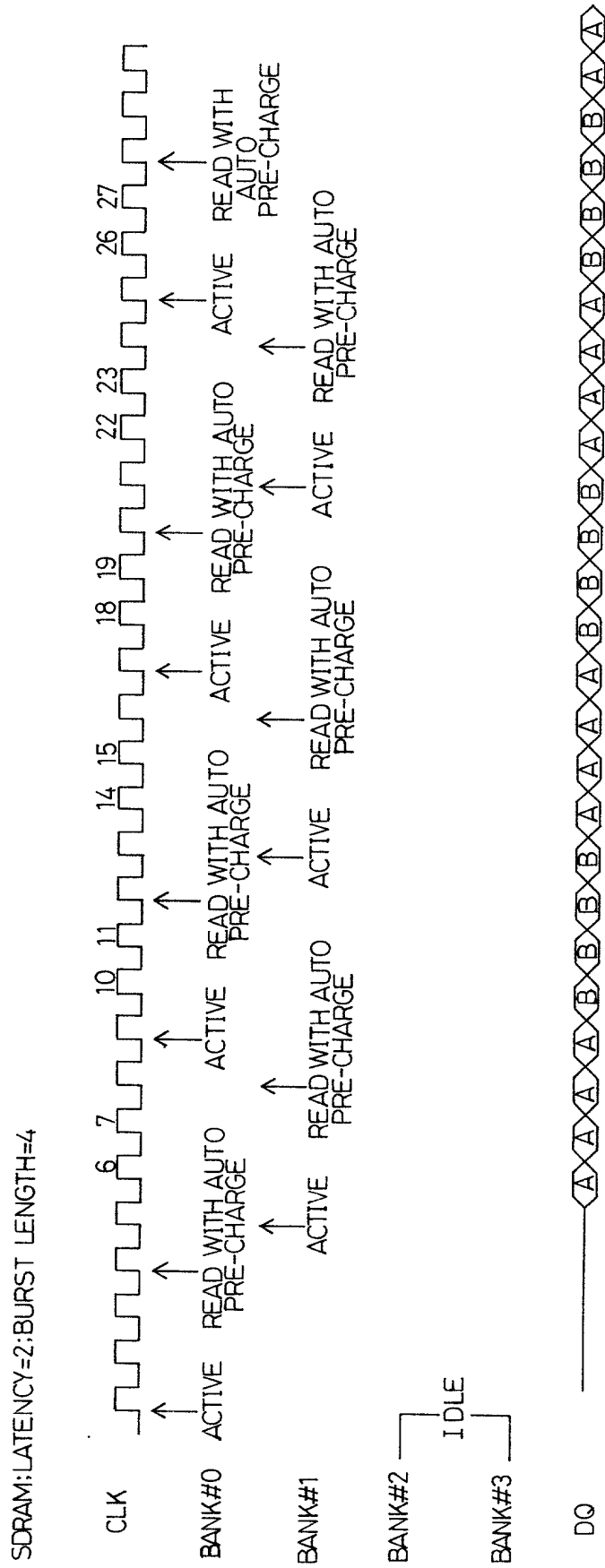


FIG. 10A
PRIOR ART

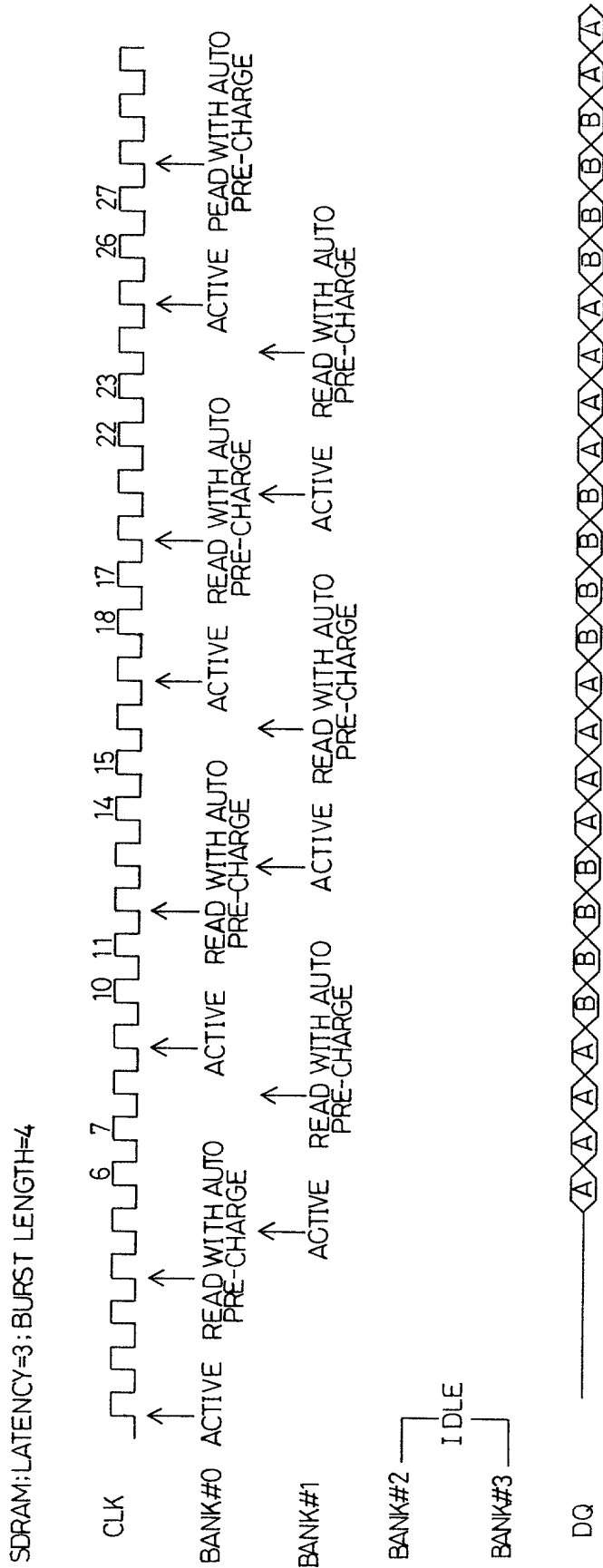


FIG. 10B
PRIOR ART

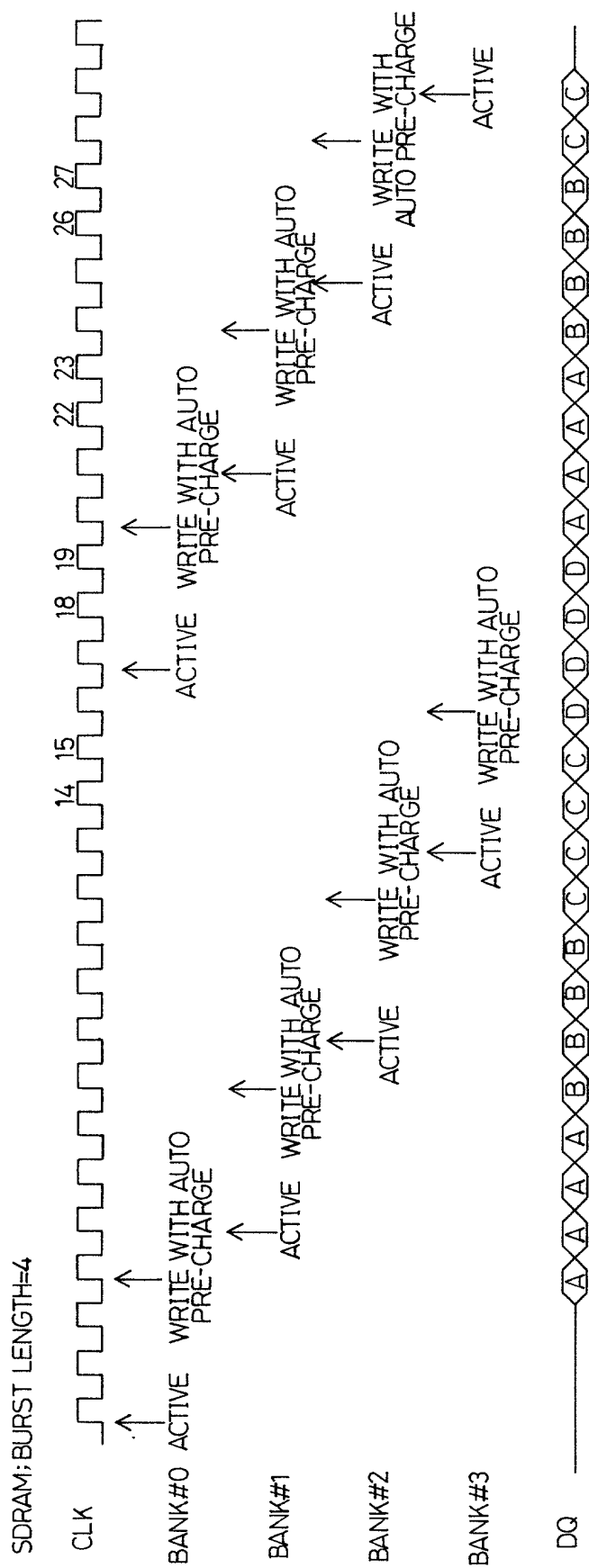


FIG. 11
PRIOR ART

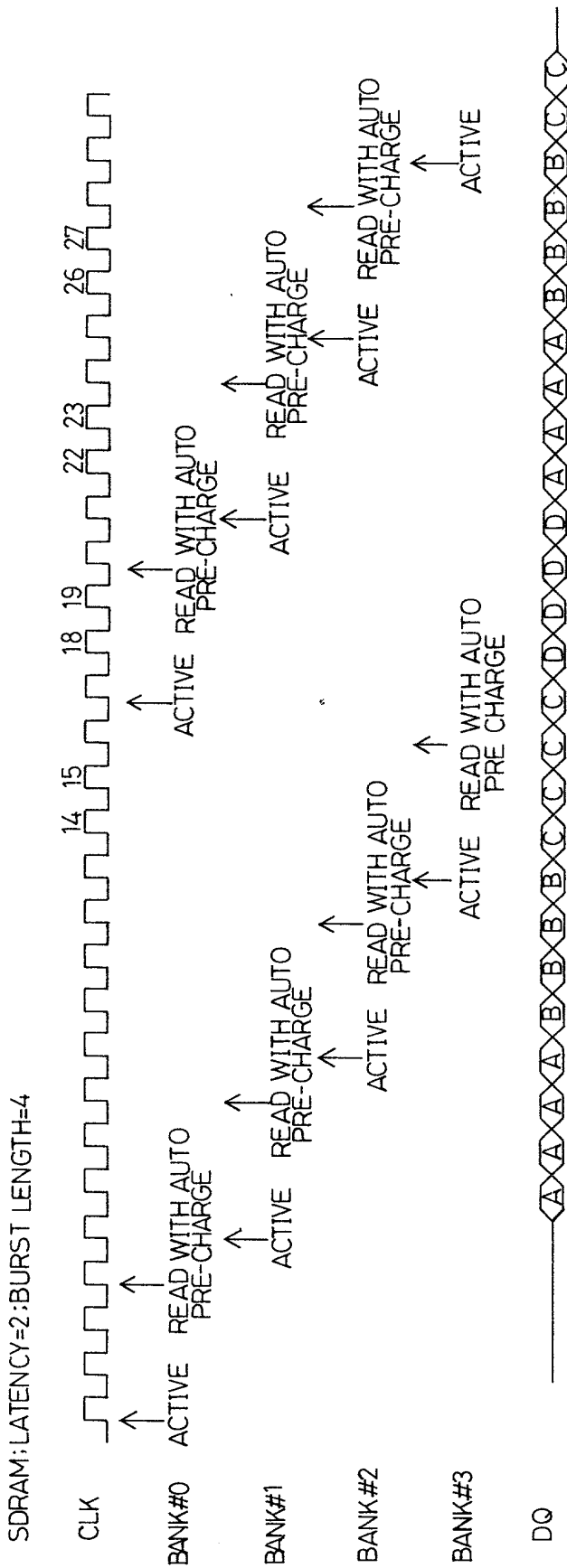


FIG.12A
PRIOR ART

SDRAM: LATENCY=3; BURST LENGTH=4

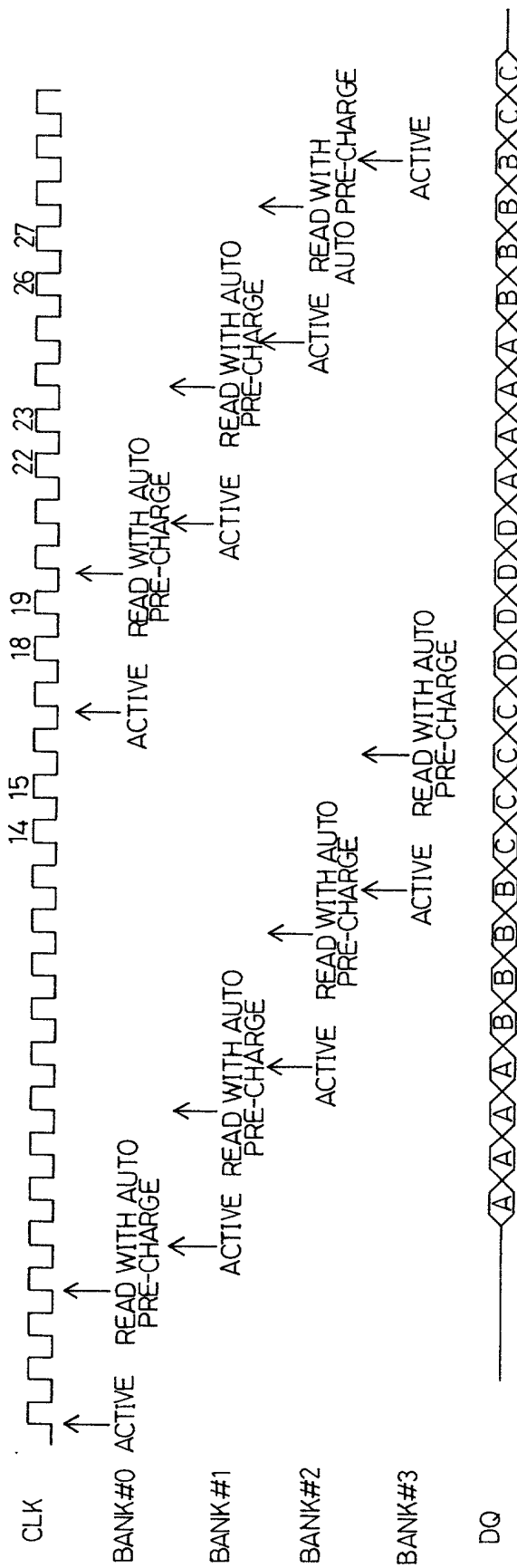


FIG. 12B
PRIOR ART